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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,735	01/16/2002	Derek Knee	10016659-1	7746

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EXAMINER	
COTTINGHAM, JOHN R	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,735	KNEE ET AL.	
	Examiner	Art Unit	
	John R. Cottingham	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 and 7-10 is/are rejected.

7)☒ Claim(s) 6 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Claim Objections

1. Claim 5 is objected to because of the following informalities: last line, the phrase "and wherein" should be removed. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Nicol et al. U.S. Patent 6,141,762.

Regarding claim 1, a multiple processor integrated circuit comprises: a first processor 101 coupled to a first cache (col. 2 lines 50-65); a first interface (calibration in Fig. 4) coupled to receive memory references that miss in the first cache; a second processor coupled to a second cache (col. 2 lines 50-65); a second interface coupled to receive memory references that miss in the second cache; common circuitry (controller) coupled to the first interface and to the second interface; a first power terminal coupled to provide power to the first processor; and a second power terminal coupled to provide power to the second processor (col. 5-6, lines 65-15).

Regarding claim 2, wherein the first interface is configured to permit operation of the second processor when the first power terminal is not powered. (col. 5, lines 41-52)

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Regarding claim 3, wherein the second interface is configured to permit operation of the first processor when the second power terminal is not powered. (col. 5, lines 41-52)

Regarding claim 4, further comprising: a third power terminal (Fig. 4) coupled to provide power to the common circuitry; and wherein the common circuitry comprises a memory bus interface.

Regarding claim 5, further comprising a third processor 103 coupled to a third cache, and a fourth processor104, coupled to a fourth cache; wherein the third processor 103 and third cache are coupled to a fourth power terminal, and the fourth processor and fourth cache are coupled to a fifth power terminal.

Regarding claim 7, a system comprising: a multiple processor integrated circuit further comprising: a first processor 101 coupled to a first cache (col. 2, lines 50-55), a first interface (configuration) coupled to receive memory references that miss in the first cache, a second processor 102 coupled to a second cache (col. 2, lines 50-55), a second interface coupled to receive memory references that miss in the second cache, common circuitry 150 coupled to the first interface and to the second interface, a first power terminal coupled to provide power to the first processor, and a second power terminal coupled to provide power to the second processor; a first power supply coupled to the first power terminal of the multiple processor integrated circuit; a second power supply coupled to the second power terminal of the multiple processor integrated circuit; and a system controller (controller) coupled to the common circuitry of the multiple processor integrated circuit, to a system memory, and I/O circuitry 160.

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Regarding claim 8, wherein the first interface of the multiple processor integrated circuit is configured to permit operation of the second processor when the first power terminal is not powered. (col. 5, lines 40-52)

Regarding claim 9, wherein the first power supply is coupled to the I/0 circuitry, and wherein the first power supply can be turned off under command of the 1/0 circuitry.

Regarding claim 10, wherein the second power supply is coupled to the I/0 circuitry, and wherein the second power supply is capable of being set to a first and a second operating voltage.

Allowable Subject Matter

3. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kabemoto et al. U.S. Patent 5,890,217, Baumgartner et al. U.S. Patent 6,108,764, Howard et al. U.S. Patent 6,711,691, Tanikawa U.S. Patent 6,035,358, and Ashida et al. U.S. Patent 6,598,108 show similar inventions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John R. Cottingham whose telephone number is (571) 272-7079. The examiner can normally be reached on Monday - Thursday, alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571)272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John R. Cottingham
Primary Examiner
Art Unit 2116

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